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Tilt-axis effect on oxidation behaviour and capacitance–voltage characteristics of (1 0 0) silicon

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(1 0 0) Si and 4° off (1 0 0) Si were oxidized in dry oxygen, and the differences in thermal oxidation behaviour, oxidation-induced stacking faults and capacitance–voltage characteristics were investigated. The thickness of the oxide produced by oxidation of the silicon samples in dry oxygen in the temperature range 1000–1200 °C was measured using an ellipsometer. The oxidation rates of the 4° off (1 0 0) Si were faster than those of the (1 0 0) Si but the differences between them decreased as the oxidation temperature increased. The size of the oxidation-induced stacking faults increased as the oxidation time and temperature increased from 1100 to 1200 °C. The density of oxidation-induced stacking faults was lower for the 4° off (1 0 0) Si than for the (1 0 0) Si. Variations in the capacitance–voltage characteristics with the oxidation temperature showed that the flat band voltages were shifted positively. The fixed surface state charge density and the interface trapped charge density of the 4° off (1 0 0) Si were lower than those of the (1 0 0) Si. Si lattice strains induced by excess interstitial Si atoms were investigated through convergent beam electron diffraction. The lattice strain of the 4° off (1 0 0) Si was lower than that of the (1 0 0) Si and this showed that the 4° off (1 0 0) Si had a lower interstitial concentration.

1. Introduction

The thermal oxidation of single crystal silicon has been extensively studied due to its role in modern integrated circuit production [1–6]. However, the thermal oxidation of silicon is known to induce the growth of stacking faults in the silicon [7–9]. The presence of these stacking faults causes adverse effects on the performance of the integrated circuit, e.g., current leakage in junction diodes and bipolar transistors, storage time degradation in MOS devices, etc. [10–12]. In addition, charges are present in oxidized silicon structures and these adversely affect junction leakage, noise, and the breakdown voltage in discrete transistors and integrated circuits, and device stability in MOS devices [13]. The concentration of oxidation-induced stacking faults can be reduced by a heat treatment at high temperatures in a nonoxidizing atmosphere such as Ar or by oxidation with chlorine species [14, 15]. In addition, silicon wafers that display orientations inclined with respect to the (1 0 0) plane at an angle between 3–10° either along the [011] or [0 1 0] zone have been reported to show a considerably reduced stacking fault content [16]. The oxide charge content can be minimized by additional treatments such as annealing in an inert or an hydrogen atmosphere [17, 18]. For future developments, more highly integrated, reliable, and reproducible devices are needed, and thus better control of the substrate characteristics as well as the oxide layer properties are required. Hence, in this study, the effect that tilting the silicon surface orientation has on the thermal oxidation behaviour, the oxidation-induced stacking fault content and the capacitance–voltage characteristics has been investigated by oxidizing (1 0 0) silicon and 4° off (1 0 0) silicon in dry oxygen. In order to provide a theoretical explanation for these effects, the lattice strain produced by silicon interstitials, that are produced due to incomplete oxidation and whose content depends on the surface orientation, were investigated using convergent beam electron diffraction methods.

2. Experimental procedure

The wafers used for this study were boron doped p-type single crystal silicon with orientations parallel to the (1 0 0) plane and inclined with respect to the (1 0 0) plane at an angle of 4° along the [0 1 0] zone. They had a resistivity of 5–8 $\Omega \times$ cm and 11 $\Omega \times$ cm, respectively. Silicon slices were cut into 1×1 cm squares and cleaned with organic solvents, etched in hydrofluoric acid and rinsed in deionized water. Specimens were placed flat in a quartz boat during oxidation and dry oxygen was supplied at 50 sccm (standard cubic centimetre). The temperature was controlled within $\pm$ 3 °C over the range 1000–1200 °C.

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The oxide thickness was determined using an ellipsometer and a scanning electron microscope.

For the optical observation of oxidation-induced stacking faults, silicon slices 2×2 cm were oxidized at 1100–1200 °C. After removal of the oxide layer by hydrofluoric acid, the surfaces were etched for 2 min by Shimmel etching [19] and examined with a metallurgical microscope.

High frequency (1 MHz) capacitance–voltage (C–V) characteristics were measured using an LF Impedance analyser over the range of -15–5 V with a sweep speed of 0.2 V s^{-1}. Gate and back side electrodes were produced by evaporating aluminium at 4×10^{-3} Pa onto the specimens oxidized at 1000–1200 °C to produce an oxide thickness of 57 nm (± 1.5 nm). The flat band voltages and oxide charges were calculated from the measured C–V characteristics.

To measure the silicon lattice strain after oxidation, each wafer was oxidized at 1200 °C for 3 h and the silicon lattice parameter variations from the Si/SiO_2 interface were compared using convergent beam electron diffraction on samples with and without an oxide layer. The examination was performed at an accelerating voltage of 100 kV and [0 1 2] HOLZ zone axis patterns were used since small deviations from true dynamic diffraction conditions prevail at lower symmetry zone axis, allowing accurate computer simulation. Computer simulation using the program DIFFRACT were performed to find the corrected accelerating voltage value for the reference sample (unoxidized silicon) and also to estimate the lattice parameter of the silicon substrate as a function of distance away from the interface.

3. Results and discussion

3.1. Thermal oxidation of silicon

The oxidation rate of silicon depends on the crystallographic orientation of the surface plane, that is, the number of available bonds in the silicon crystal plane [20, 21]. If the surface plane normal is tilted away from [1 0 0] by 4° towards [0 1 0], the density of surface steps and kinks increases due to the atomic structure of silicon and in addition the number of available bonds increases [12]. The number of available bonds in the (1 0 0) and (1 1 0) planes are reported to be 6.8×10^{14} cm^{-2} and 9.6×10^{14} cm^{-2}, respectively [20]. From these values, the number of available bonds for the 4° off (1 0 0) plane were calculated to be 7.45×10^{14} cm^{-2}. Thus, as is shown in Fig. 1, the oxidation rate of the 4° off (1 0 0) silicon was more rapid than the (1 0 0) silicon. Very little difference in the rates was noted at 1200 °C. However, at 1000 °C, the (1 0 0) values were definitely lower than those of the 4° off (1 0 0). This is because the oxidation rates in the linear growth region, in which the growth rate is limited by the reaction at the Si/SiO_2 interface, of the 4° off (1 0 0) plane were more rapid than those of the (1 0 0) plane owing to the difference in the number of available bonds. This could be ascertained by the result that a detailed plot of oxide thickness versus time did not extrapolate to a zero initial thickess. Also, the oxidation rate of silicon depends on the impurity

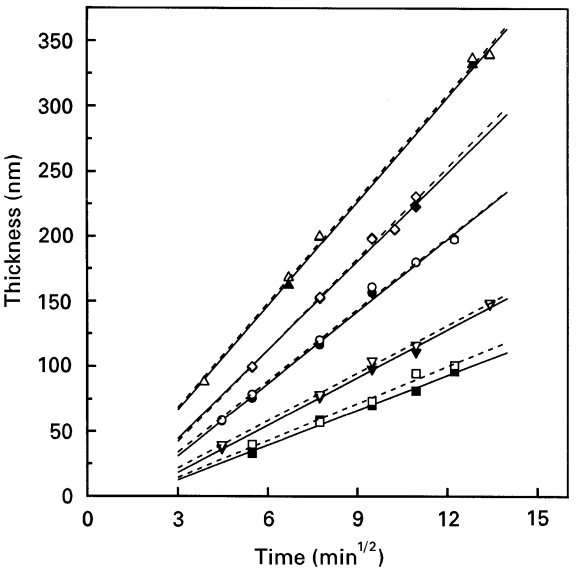

Figure 1 A comparison of the oxidation results for (1 0 0) and 4° off (1 0 0) Si in dry O_2; solid lines, solid symbols – (1 0 0) Si, dashed lines, open symbols - 4° off (1 0 0) Si. The temperatures investigated were: (□, ■) 1000 °C; (▼, ▽) 1050 °C; (●, ○) 1100 °C; (◆, ◇) 1150 °C and (▲, △) 1200 °C.

doping concentration [20, 22] and thus the oxidation rate of (1 0 0) silicon with an impurity concentration of 1.6–2.6×10^{15} atoms cm^{-3} should be more rapid than that of the 4° off (1 0 0) silicon with an impurity concentration of 1×10^{15} atoms cm^{-3} [23]. However, the opposite results were observed, which apparently further highlights the effects of the crystal orientation.

Linear and parabolic rate constants for oxidation were calculated as follows. The initial condition $x_i = 23.0$ nm and the corresponding values of $\tau \equiv (x_i^2 + Ax_i)/B$ were adopted from reference [1]. Where, x_i, x_0, B, B/A and τ are called the initial thickness of oxide on silicon, the thickness of oxide, the parabolic rate constant, the linear rate constant and a shift in the time coordinate to account for the presence of the initial thickness of oxide on silicon, respectively. From the plot of x_0 versus $(t + \tau)/x_0$, the slopes of the lines corresponded to B and the intercepts at $(t + \tau)/x_0 = 0$ corresponded to $-A$ in the equation

$$x_0^2 + Ax_0 = B(t + \tau). \quad (1)$$

With the resulting A and B, τ were calculated for this system and by iterating the above calculation, rate constants were evaluated. The resulting rate constants for dry oxygen are listed in Table I. The logarithms of the parabolic rate constant, B and the linear rate constant, B/A are plotted in Fig. 2 against the reciprocal of the absolute temperature. The linear rate constants, B/A of the 4° off (1 0 0) silicon were generally larger than those of the (1 0 0) silicon, which closely agrees with the preceding explanation of the effect of the number of available bonds. The activation energies of B for the (1 0 0) and 4° off (1 0 0) silicon samples were found to be 107.9 and 119.7 kJ mol^{-1} respectively. These are similar to the value of 119.2 kJ mol^{-1} found by Deal and Grove [1] and the 117.2 kJ mol^{-1} value reported by Norton [24] for the diffusivity of oxygen through fused silica. The activation energies of the linear rate constant, B/A for the (1 0 0) and 4° off

TABLE I Rate constants and activation energies for oxidation of silicon in dry oxygen. $x_0^2 + Ax_0 = B(t + \tau)$

	Oxidation temperature (°C)	A (μm)	B (μm^2 h^{-1})	B/A (μm h^{-1})	τ (h)	E_B (kJ mol^{-1})	$E_{B/A}$ (kJ mol^{-1})
Reference [1]	1000	0.165	0.0117	0.071	0.37		
	1100	0.090	0.027	0.30	0.076	119.2	192.5
	1200	0.040	0.045	1.12	0.027		
	1000	0.2356	0.011	0.047	0.541		
(1 0 0) Si	1100	0.1075	0.0245	0.228	0.123	107.9	237.7
	1200	0.0438	0.044	1.005	0.035		
	1000	0.1630	0.0095	0.058	0.45		
4° off (1 0 0) Si	1100	0.0914	0.0233	0.255	0.113	119.7	229.7
	1200	0.0393	0.0442	1.125	0.032		

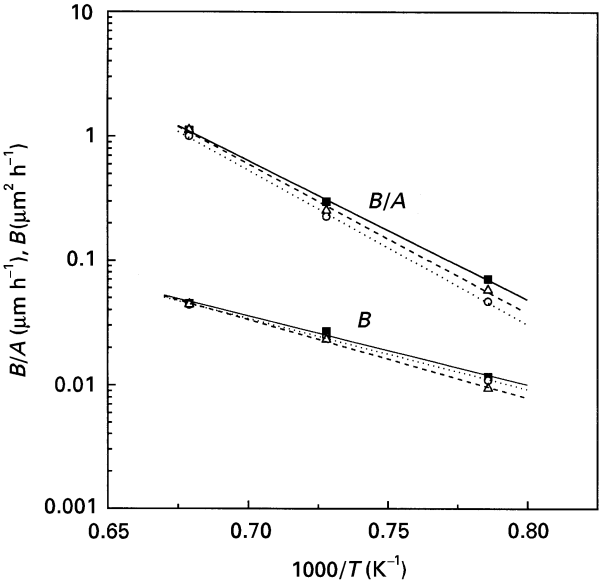

Figure 2 The effect of temperature on the linear rate constant, B/A and the parabolic rate constant, B. Key: (■) Deal and Grove [1]; (○) (1 0 0) Si and (△) 4° off (1 0 0) Si.

(1 0 0) silicon samples were 237.7 and 229.7 kJ mol^{-1}, respectively which are different from the 192.5 kJ mol^{-1} of Deal and Grove [1] and the 176.6 kJ mol^{-1} required to break a Si–Si bond [20].

3.2. Oxidation-induced stacking faults

The thermal oxidation of silicon creates excess interstitial silicon atoms near the Si/SiO_2 interface. Some atoms can escape into the bulk silicon and become silicon self-interstitials while others flow into the bulk oxide and quickly react with incoming oxygen near the interface. A supersaturation of silicon interstitials occurs in the silicon substrate near the Si/SiO_2 interface an oxidation-induced stacking faults (OSF) grow by absorbing these interstitials [7–9].

There exists a certain density of active sites on the silicon surface. These sites are kinks in the surface steps and the density of these kinks is strongly dependent on surface orientation. Hu [8] has reported that when the excess interstitials, are in the neighbourhood of these kinks, they are captured by the kinks and undergo a surface regrowth. Thus the rate of surface regrowth is directly proportional to the surface kink density. Hence, the concentration of excess interstitials will be a decreasing function of the kink density and consequently will depend on the surface orientation. Therefore, the growth of OSF (size as well as density) is dependent on the kink density and the crystal orientation of the silicon surface. Oxidation-induced stacking faults were not observed to occur at temperatures below 950 °C [13] and so their growth as a function of oxidation time and temperature in the range 1100–1200 °C is investigated in the present work. Fig. 3 shows the growth of the stacking faults as the oxidation temperature increases and Fig. 4 shows the time dependence of the OSF growth when silicon is oxidized at 1200 °C. The densities of OSF on (1 0 0) and 4° off (1 0 0) silicon samples oxidized at 1150 °C were about 4.2×10^7 and 3.8×10^6 cm^{-2} respectively. Therefore, considerable decreases in the density and the size of OSF for the 4° (1 0 0) silicon were observed over the experimental range.

The thermal oxidation of silicon produces stacking faults lying on {1 1 1} planes. Therefore, stacking fault traces on the (1 0 0) surface form right angles with these faults but those on the 4° off (1 0 0) surface will

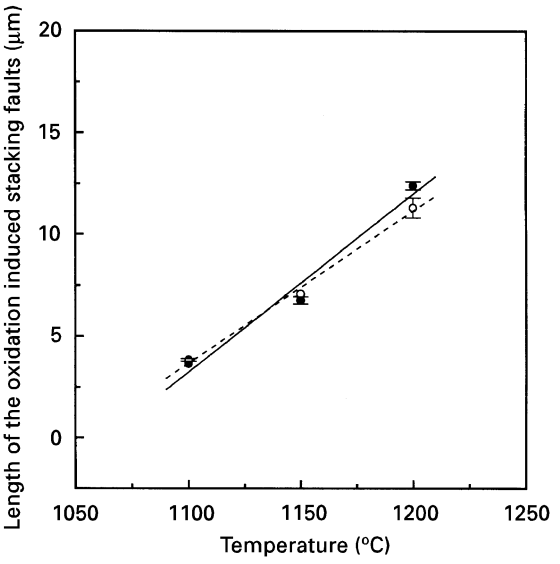

Figure 3 Variation of the size of the oxidation-induced stacking faults as a function of oxidation temperature. The oxidation time was 180 min for (●) (1 0 0) Si and (○) 4° off (1 0 0) Si.

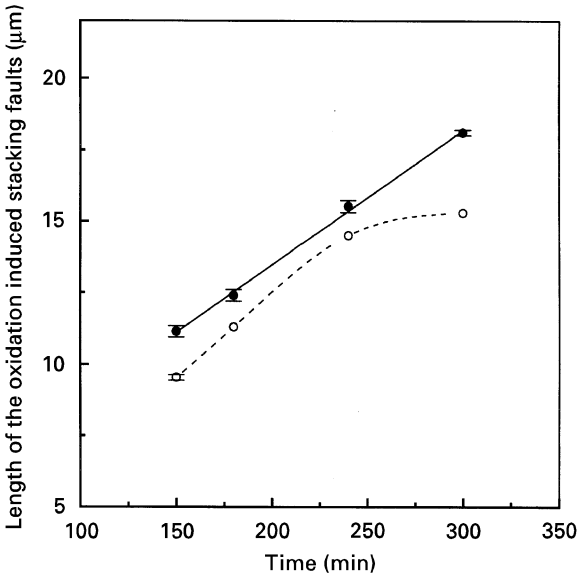

Figure 4 Variation of the size of the oxidation-induced stacking faults produced at 1200 °C as a function of oxidation time for (●) (1 0 0) Si and (○) 4° off (1 0 0) Si.

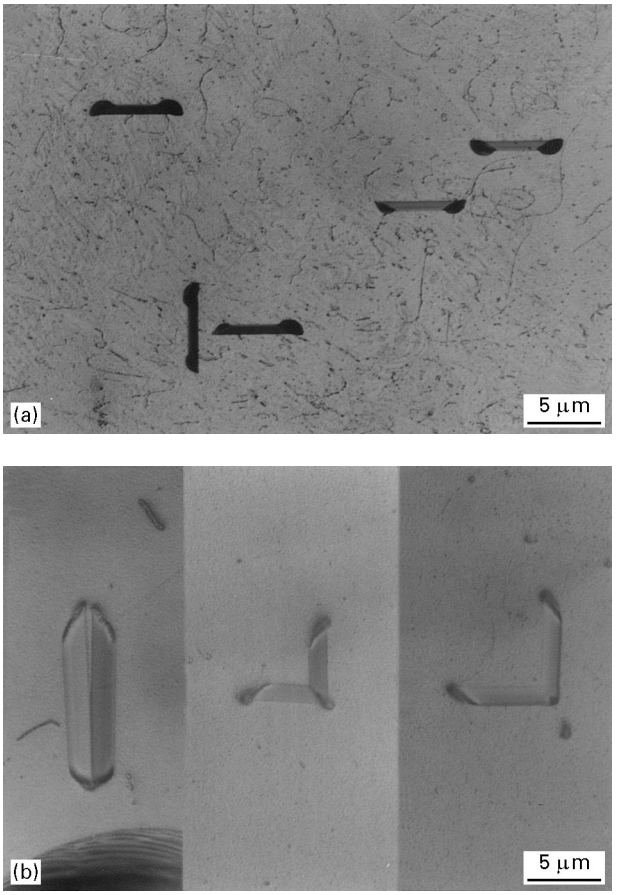

Figure 5 Oxidation-induced stacking faults having various angles on the surface of (a) (1 0 0) Si and (b) 4° off (1 0 0) Si wafers.

deviate from the right angle. The calculated angles were 93.7, 85.7 and 4° which closely agree with the observed angles shown in Fig. 5(a and b).

3.3. Capacitance–voltage characteristics

In order to examine the effects of silicon crystal orientation and OSF on the application of MOS devices,

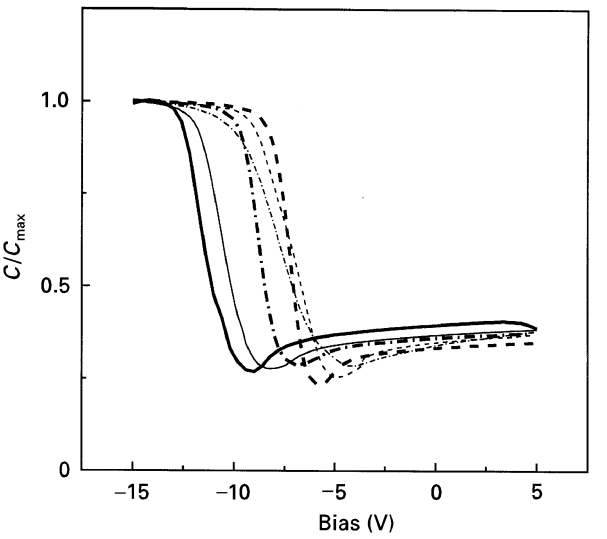

Figure 6 Measured C–V characteristics after dry oxidation at temperatures of (—) 1000 °C, (–·–·) 1100 °C and (– – –) 1200 °C. Thin lines – (1 0 0) Si, thick lines – 4° of (1 0 0) Si.

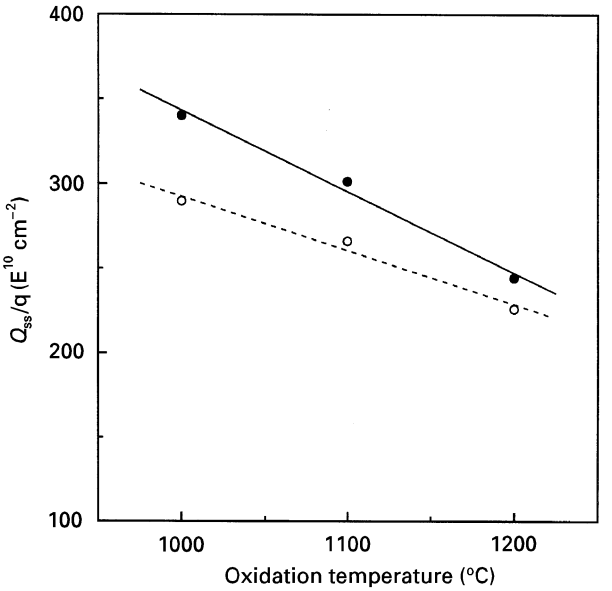

Figure 7 Fixed surface state charge densities after dry oxidation for (●) (1 0 0) Si and (○) 4° off (1 0 0) Si.

capacitance–voltage (C–V) characteristics were investigated. Measured C–V curves are shown in Fig. 6. The flat band voltages, V_{FB} were shifted positively as the oxidation temperature increased. This effect is caused by the fact that the fixed surface state charge, Q_{SS} and the interface trapped charge, Q_{IT} decreased as the oxidation temperature increased [16]. The origins of these oxide charges, Q_{SS} and Q_{IT} are respectively excess ionic silicon in the vicinity of the Si/SiO_2 interface that has broken away from the silicon and unsatisfied chemical bonds (so-called "dangling bonds") at the surface of silicon. These charge densities depend on the silicon surface orientation and are greatest on {1 1 1} Si surfaces and smallest on {1 0 0} surfaces [13, 18, 25]. In this study, on the contrary, the Q_{SS} on the 4° off (1 0 0) surfaces was lower than that on the (1 0 0) surfaces as is shown in Fig. 7 despite the fact that the

number of available silicon bonds for the 4° off (1 0 0) surface is larger than that for the (1 0 0) surface. Also, the interface trapped charge induces the distorted or spread out nature of the C–V characteristics. In Fig. 6, the C–V curves of 4° off (1 0 0) Si spread out less than those of (1 0 0) Si and so Q_{IT} of the 4° off (1 0 0) Si could be inferred to be lower than that of (1 0 0) Si. These contradictory results are thought to originate from the fact that the structural kinks on the 4° off (1 0 0) surface lower the excess silicon interstitial concentrations and thus, lower the oxide charge densities as well as the growth of OSF.

3.4. Lattice strain measurement through convergent beam electron diffraction

Lattice strain in silicon consists of two components, one called intrinsic that is generated during the high temperature oxidation process due to a density difference between Si and SiO_2 at the growth temperature and secondly the incorporation of Si interstitials into the silicon lattice. The second component is introduced during cooling to room temperature due to a thermal expansion mismatch between the Si and SiO_2. The measured lattice strain in silicon with an oxide layer reflects the sum of intrinsic and thermal strain, while the removal of the oxide layer will leave only the contribution from the intrinsic strain.

In order to measure the lattice strain or the concentration of silicon interstitials in silicon during high temperature oxidation, variations of the lattice parameter from the Si/SiO_2 interface were compared through the convergent beam electron diffraction (CBED) method after the removal of the oxide layer. Fig. 8 shows a [0 1 2] higher order Laue zone (HOLZ) pattern whilst Fig. 8b shows the pattern simulated with a lattice parameter, $a = 0.54309$ nm and an accelerating voltage, $E_a = 100$ kV. The [0 1 2] zone axis was chosen for two reasons. Firstly, the errors from dynamic electron diffraction are small for low symmetry zone axis such as the [0 1 2] and secondly, by choosing this zone axis, the sample could be tilted from [0 1 1] to [0 1 2] with a small tilt angle parallel to the interface. This minimizes the effect of thickness variations in a tilted sample. The typical probe size used in the experiment was 50 nm. Comparing the simulated pattern with the experimental one from the Si standard, the corrected accelerating voltage values, 100.2 kV for a/b (strain parallel to the interface) and 100.4 kV for c/d (strain perpendicular to the interface) were found from the simulation of the HOLZ patterns. This correction is essential for the compensation of the error accompanying the kinematic approximation of electron diffraction pattern simulation. With these corrected accelerating voltages, the variation of the silicon lattice parameter as a function of distance away from the Si/SiO_2 interface were measured from the [0 1 2] experimental HOLZ patterns. As is shown in Fig. 9a, the strain profile in oxidized silicon exhibits a slowly diminishing trend and approaches zero about 2.5 μm from the interface. When the oxide layer was removed, the strain increased at the interface to 3.15×10^{-3} and then decreased sharply to zero at 1.0 μm from the interface. Fig. 9b shows both the intrinsic and thermal components of the lattice strain in silicon. It is interesting to note that the thermal strain in silicon very close to the interface is in compression and becomes zero at about 0.4 μm and changes to tensile strain further away from the interface. Since the thermal expansion coefficient of silicon is five times larger than that of SiO_2, tensile thermal strain is expected in silicon. The existence of a compressive thermal strain in silicon near the interface region is believed to be the effect of a high silicon interstitial concentration that modifies the local thermal expansion coefficient of silicon to a level lower than that of SiO_2. This hypothesis is further supported by the evidence that the sign of the thermal strain changes with the magnitude of intrinsic strain in silicon as is shown in Fig. 9b.

Without the oxide layer, the intrinsic strain in (1 0 0) silicon was 3.15×10^{-3} and for 4° off (1 0 0) silicon it was 1.75×10^{-3} at a position 0.1 μm away from the interface. The magnitude of the strain in the 4° off silicon is much lower than that of the (1 0 0) silicon confirming that the concentration of interstitial silicon

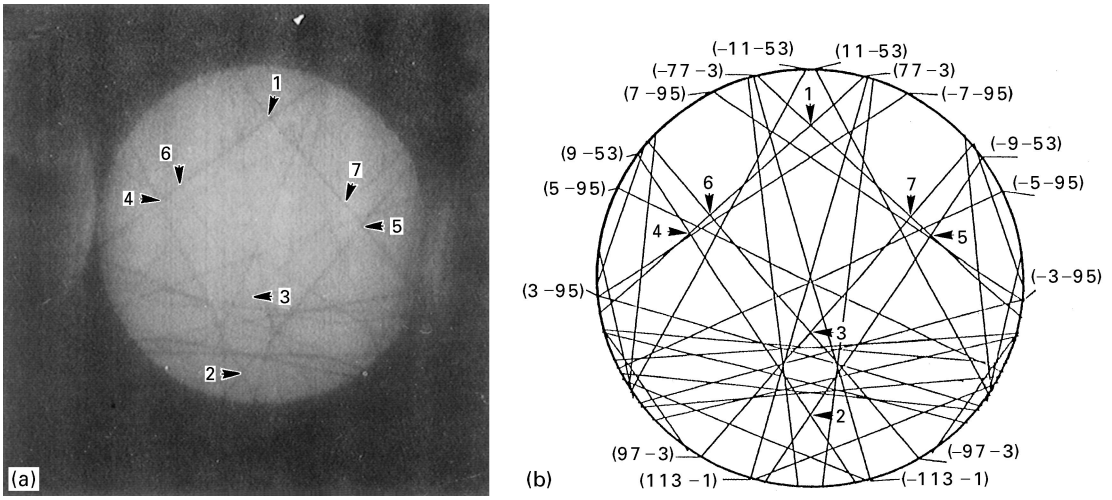

Figure 8 (a) [0 1 2] HOLZ pattern for Si at an accelerating voltage, E_a of 100 kV. (b) Pattern simulated with a Si lattice parameter of $a_0 = 0.54309$ nm. a, b, c, d indicate the lengths between the points, i.e., a: 12, b: 13, c: 45, d: 67.

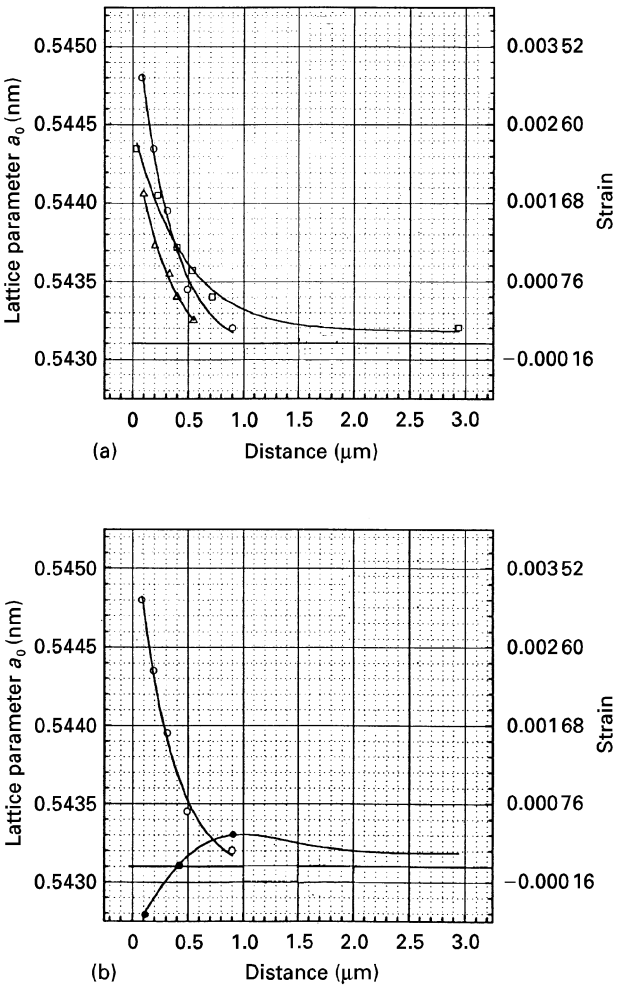

Figure 9 The lattice parameter variations and strain profiles in (1 0 0) Si and 4° off (1 0 0) Si, (a) strain profiles of silicon as a function of distance from the interface for (□) (1 0 0) Si with oxide; (○) (1 0 0) Si and (△) 4° off (1 0 0) Si and (b) (○) intrinsic and (●) thermal strain in (1 0 0) Si. Note that the standard lattice parameter is $a = 0.54309$ nm.

is significantly higher in (1 0 0) silicon. This result obtained from lattice strain measurements by CBED verifies the previous explanation of the structural kink effects on the oxidation behaviour, oxidation-induced stacking faults, and C–V characteristics.

4. Summary and conclusions

Tilt-axis effects on the thermal oxidation behaviour, oxidation-induced stacking faults and capacitance–voltage characteristics of silicon were investigated by oxidizing (1 0 0) silicon and 4° off (1 0 0) silicon in dry oxygen. The oxidation rates of the 4° off (1 0 0) silicon were more rapid than those of the (1 0 0) silicon over the range of 1000–1200 °C and the difference decreased as the oxidation temperature increased. This is because oxidation rates in the linear growth region, in which the growth rate is limited by reaction at the Si/SiO_2 interface, are more rapid for 4° off (1 0 0) planes than for (1 0 0) planes. This is because of a difference in the number of available bonds. The activation energies based on the parabolic rate constant, B for the (1 0 0) and 4° off (1 0 0) Si were 107.9 and 119.7 kJ mol^{-1} and those on the linear rate constant, B/A were 237.7 and 229.7 kJ mol^{-1}, respectively. Considerable decreases in the size and the density of OSF for 4° off (1 0 0) silicon were observed in the range 1100–1200 °C. Flat band voltages estimated from the C–V curves shifted positively as the oxidation temperature increased which is caused by the fact that the fixed surface state charge, Q_{SS} and the interface trapped charge, Q_{IT} decrease with increasing oxidation temperature. The Q_{SS} and Q_{IT} of the 4° off (1 0 0) silicon were lower than those of the (1 0 0) silicon inspite of the larger number of available silicon bonds. These results can be explained by a mechanism in which structural kinks on the 4° off (1 0 0) surface capture excess silicon interstitials thereby lowering the interstitial concentration and thus, lower the oxide charge densities as well as the growth of OSF. This proposal is consistent with measurements of the silicon lattice strain made by convergent beam electron diffraction.

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References

1. B. E. DEAL and A. S. GROVE, *J. Appl. Phys.* **36** (1965) 3770.
2. B. E. DEAL, *J. Electrochem. Soc.* **110** (1963) 527.
3. R. H. DOREMUS, *J. Phys. Chem.* **80** (16) (1976) 1773.
4. R. L. MEEK, *J. Amer. Ceram. Soc.* **56** (1973) 341.
5. N. S. JACOBSON, *ibid.* **76** (1993) 3.
6. W. A. TILLER, *J. Electrochem. Soc.* **127** (1980) 619.
7. A. M. LIN, R. W. DUTTON, D. A. ANTONIADIS and W. A. TILLER, *ibid.* **128** (1981) 1121.
8. S. M. HU, *J. Appl. Phys.* **45** (1974) 1567.
9. *Idem., Appl. Phys. Lett.* **27** (1975) 165.
10. S. KAWADO, *Jpn J. Appl. Phys.* **19** (1980) 1591.
11. K. V. RAVI, C. J. VARKER and C. E. VOLK, *J. Electrochem. Soc.* **120** (1973) 533.
12. J. KANIEWSKI, M. KANIEWSKA and A. R. PEAKER, *Appl. Phys. Lett.* **60** (1992) 359.
13. B. E. DEAL, *J. Electrochem. Soc.* **121** (1974) 198C.
14. T. HATTORI and T. SUZUKI, *Appl. Phys. Lett.* **33** (1978) 347.
15. T. HATTORI, *J. Electrochem. Soc.* **123** (1976) 945.
16. Y. SUGITA, T. GATO and M. TAMURA, *J. Appl. Phys.* **42** (1971) 5847.
17. R. F. PIERRET, in "Modular series on solid state devices – Vol. IV: Field effect devices", edited by G. W. Neudeck and R. F. Pierret, (Addison-Wesley, MA. 1990) p. 103.
18. B. E. DEAL, *IEEE Trans. Electron Devices* **ED-27** (1980) 606.
19. D. G. SCHIMMEL, *J. Electrochem. Soc.* **126** (1979) 479.
20. S. M. SZE, "VLSI technology", (McGraw-Hill, New York, 1988) p. 98.
21. J. R. LIGENZA, *J. Phys. Chem.* **65** (1961) 2011.
22. R. C. JAEGER, in "Modular series on solid state devices – Vol. V: Introduction to microelectronic fabrication", edited by G. W. Neudeck and R. F. Pierret, (Addison-Wesley, MA, 1990) pp. 29–46.
23. R. F. PIERRET, in "Modular series on solid state devices – Vol. I: Semiconductor fundamentals", edited by G. W. Neudeck and R. F. Pierret, (Addison-Wesley, MA. 1989) p. 71.
24. F. J. NORTON, *Nature* **191** (1961) 701.
25. "Principles and models of semiconductor devices", (Stanford University, Stanford CA, 1988) p. 339.

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